

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

EVERETT LEE

Application No.:

Filed:

For: **Contact-Layout For Flash Memory Array**

Art Group:

Examiner:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In accordance with the duty of disclosure, enclosed is a copy of Information Disclosure Statement by Applicant (form PTO/SB/08), which is being submitted concurrently with the Utility Application. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

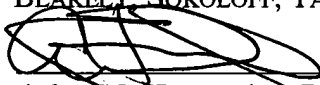
The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: December 31, 2003


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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



Carla Vignola

12-31-03

Date

Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	
				Filing Date	
				First Named Inventor	Everett Lee
				Art Unit	
				Examiner Name	
Sheet	1	of	1	Attorney Docket Number	42P18035

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T ²
		KIM, J., et al., "A Novel 4.6F2 NOR Cell Technology With Lightly Doped Sourd (LDS) Junction For High Density Flash Memories," IEEE, 1998, 4 pages,		
		Memory Division, Samsung Electronics Co., LTD.		
		PAVAN, P., et al., "Flash Memory Cells-An Overview," IEEE, 1997, Vol. 85, No. 8, August 1997, pages 1248-1271.		

Examiner Signature		Date Considered	
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*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Applicant's unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.

Based on PTO/SB/08B (08-03) as modified by Blakely, Solokoff, Taylor & Zalman (wlr) 08/11/2003.
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